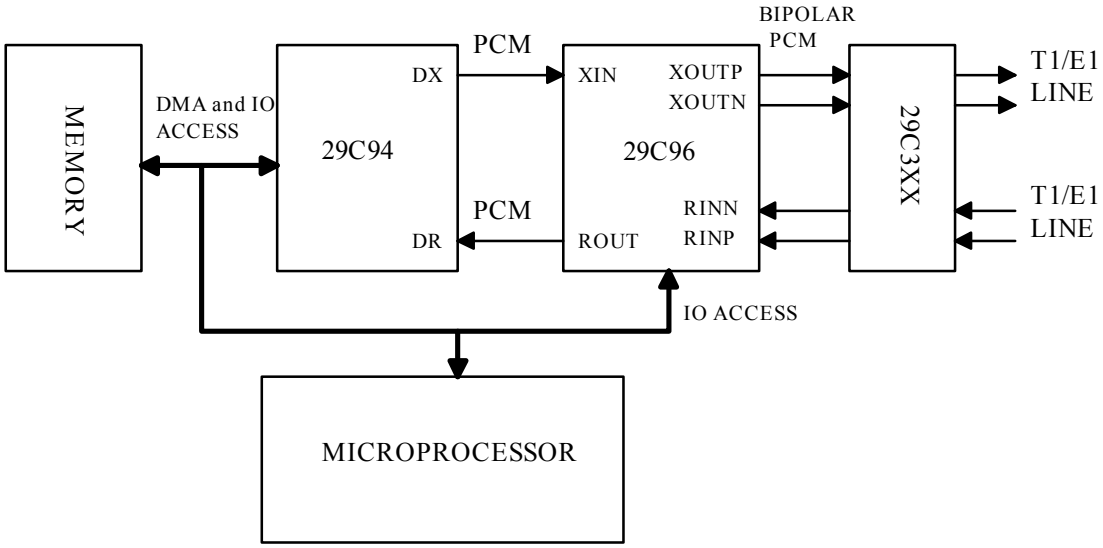
Connecting 29C96 and 29C94

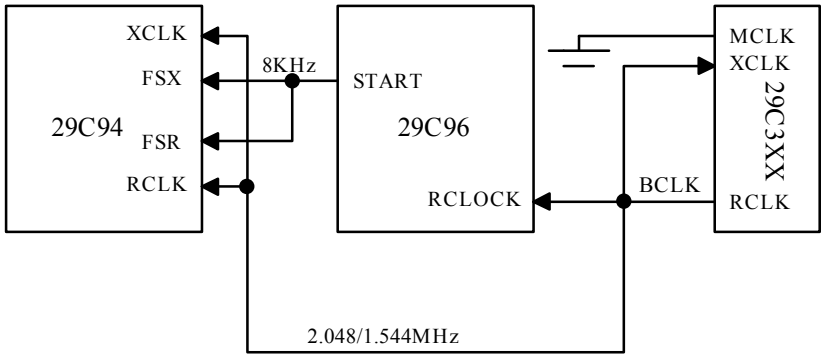
Introduction

The 29C94 and 29C96 are parts of MHS's ISDN primary rate chipset. The 29C94 is a multichannel HDLC controller and the 29C96 is a framer with time slots switching capabilities. These two components can be used in T1-DS1 (1.544MHz) or E1-CEPT (2.048MHz) mode. A 29C3xx transceiver will be added to these two components to form the ISDN chipset.

ISDN Chipset Data Block Diagram



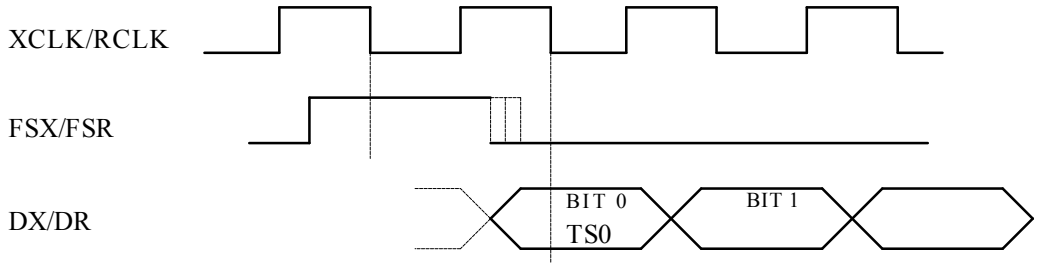
Typical Clock Block Diagram



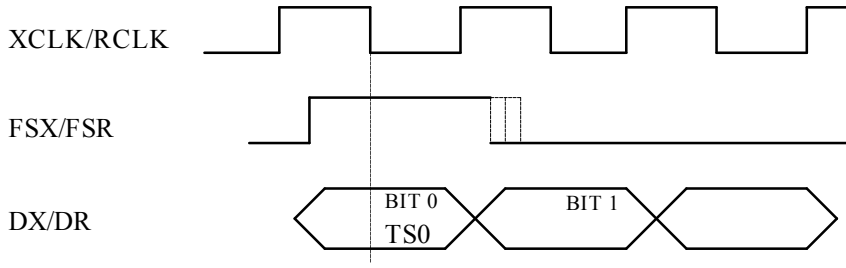
The two previous schematics show a typical data and clock connection between 29C94 and 29C96.

- data connection : the PCM line out (DX) from the 29C94 will be connected to one of the four PCM line in of the 29C96 (XIN[0..3]). One of the PCM line out (ROUT[0..3]) of the 29C96 will be connected to the PCM line in (DR) of the 29C94.
- clock connection : the bit clock (2.048MHz or 1.544MHz) will be extracted from the line by the 29C3XX and provided to the 29C96 and 29C94. To generate the Frame Synchronization Clock (8KHz), two possibilities can be used : the first one and the most common will use the free-running capability of the 29C96. The FSC signal is derivated from the bit clock provided by the 29C3XX to the 29C96 and the 29C94 is placed in slave mode. The second one is to use the Master mode of the 29C94 and place the 29C96 in slave mode. The FSC signal is derivated from the bit clock provided to the 29C94.
  - free-running mode : this mode is enabled by setting PMR.FRUN to one (see 29C96 Datasheet).
  - master mode : this mode is enabled by setting

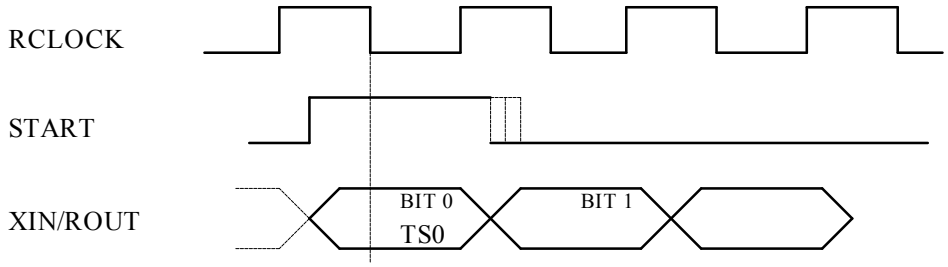
Timings diagram of 29C94 PCM line (E1 - slave mode)



Timings diagram of 29C94 PCM line (T1 - slave/master mode)



Timing diagram of 29C96 PCM line (E1-T1 mode)



- In E1 mode : these previous schematics show that bit0 of TS0 sent by the 29C94 (in slave mode) will be considered by the 29C96 as bit1 of TS0 if the natural values into R/XOFFSET are conserved (08H,0AH). To compensate the one bit clock delay between data coming from 29C94 and those expected by the 29C96, new values into R/XOFFSET will be introduced. These values will be : 09H for ROFFSET and 0BH for XOFFSET. If the 29C94 is used in master mode, the natural offsets (08H, 0AH) will be conserved
- In T1 mode : The schematics show that the natural values (08H, 0AH) introduced into R/XOFFSET will be conserved because the bit0 of TS0 is provided by the 29C94 (slave or master mode) at the same time than FSC signal. So, there is no bclk delay intoduced between data provided by the 29C94 and those expected by the 29C96.

Additional Information

For additional information please refer to 29C94 and 29C96 datasheets.